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WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory comprising:

a semiconductor substrate;

a first transistor formed on a surface of said semiconductor substrate and including a first gate insulating film and a first gate electrode; and

a second transistor formed on the surface of said semiconductor substrate and including a second gate insulating film and a second gate electrode,

wherein said first gate insulating film includes a charge storage layer and said second gate insulating film does not include a charge storage layer, and

said first and second transistors are isolated by a trench and said charge storage layer in said first transistor does not exist in an element isolation region and exists only below said first gate electrode in an element region.

2. A memory according to claim 1, wherein

said first gate insulating film comprises a 1- to 10-nm thick bottom silicon oxide film, a 0.5- to 7-nm thick silicon nitride film as said charge storage layer, and a 5- to 15-nm thick top silicon oxide film, and

the film thickness of said bottom silicon oxide film is smaller than that of said top silicon oxide film.

3. A memory according to claim 1, wherein

said first gate insulating film comprises a 1- to 10-nm thick bottom silicon oxide film, a tantalum oxide film as said charge storage layer, and a 5- to 15-nm thick top silicon oxide film, and

the film thickness of said bottom silicon oxide film is smaller than that of said top silicon oxide film.

4. A memory according to claim 1, wherein

said first gate insulating film comprises a 1- to 10-nm thick bottom silicon film, a film selected from the group consisting of a strontium titanate film and a barium strontium titanate film as said charge storage layer, and a 5- to 15-nm thick top silicon oxide film, and

the film thickness of said bottom silicon oxide film is

smaller than that of said top silicon oxide film.

5. A memory according to claim 1, wherein

said nonvolatile semiconductor memory has a cell array which comprises said first transistor as a cell transistor and said second transistor as a selection transistor, and

said second gate insulating film in said second transistor has a 5- to 15-nm thick silicon oxide film.

6. A memory according to claim 1, wherein

said nonvolatile semiconductor memory comprises peripheral transistors in a peripheral region of said cell array,

said peripheral transistors include:

a first peripheral transistor formed on the surface of said semiconductor substrate and including a third gate insulting film and a third gate electrode; and

a second peripheral transistor formed on the surface of said semiconductor substrate and including a fourth gate insulating film and a fourth gate electrode, and

said third and fourth gate insulating films have different film thicknesses.

7. A method of fabricating a nonvolatile semiconductor memory having a cell array including a cell transistor and a selection transistor, comprising the steps of:

forming a first insulating film including a charge storage layer, on a surface of a semiconductor substrate, as a gate insulating film of the cell transistor;

forming a second insulating film not including a charge storage layer, on the surface of the semiconductor substrate, as a gate insulating film of the selection transistor; and

performing element isolation by forming a trench between an element region in which the cell transistor is to be formed and an element region in which the selection transistor is to be formed,

wherein the charge storage layer in the cell transistor does not exist in an element isolation region and exists only below said first gate electrode in the element region.

8. A method according to claim 7, wherein the first gate insulating film is formed by stacking a 1- to 10-nm bottom silicon

oxide film, a 0.5- to 7-nm thick silicon nitride film as the charge storage layer, and a top silicon oxide film whose film thickness is 5 to 15 nm and not less than that of the bottom silicon oxide film.

9. A method according to claim 7, wherein the first gate insulating film is formed by stacking a 1- to 10-nm bottom silicon oxide film, a tantalum oxide film as the charge storage layer, and a top silicon oxide film whose film thickness is 5 to 15 nm and not less than that of the bottom silicon oxide film.

10. A method according to claim 7, wherein the first gate insulating film comprises a 1- to 10-nm thick bottom silicon film, a film selected from the group consisting of a strontium titanate film and a barium strontium titanate oxide film as the charge storage layer, and a top silicon oxide film whose film thickness is 5 to 15 nm and not less than that of the bottom silicon film.

11. A method according to claim 7, wherein the first and second gate insulating films include an HTO film as the topmost gate insulating layer.

12. A method of fabricating a nonvolatile semiconductor memory having a cell array including a cell transistor and a selection transistor, and a peripheral circuit including a peripheral transistor, comprising the steps of:

forming a first gate insulating film including a charge storage layer, on a surface of a semiconductor substrate, as a gate insulating film of the cell transistor;

forming a second gate insulating film not including a charge storage layer, on the surface of the semiconductor substrate, as a gate insulating film of the selection transistor;

forming a third gate insulating film not including a charge storage layer, on the surface of the semiconductor substrate, as a gate insulating film of the peripheral transistor; and

performing element isolation by forming trenches between an element region in which the cell transistor is to be formed, an element region in which the selection transistor is to be formed, and an element region in which the peripheral transistor is to be formed,

wherein the step of forming the second gate insulating film

and the step of forming the third gate insulating film are simultaneously performed, and the charge storage layer in the cell transistor does not exist in an element isolation region and exists only below said first gate electrode in the element region.

13. A method according to claim 12, wherein the first gate insulating film is formed by stacking a 1- to 10-nm bottom silicon oxide film, a 0.5- to 7-nm thick silicon nitride film as the charge storage layer, and a top silicon oxide film whose film thickness is 5 to 15 nm and not less than that of the bottom silicon oxide film.

14. A method according to claim 12, wherein the first gate insulating film is formed by stacking a 1- to 10-nm bottom silicon oxide film, a tantalum oxide film as the charge storage layer, and a top silicon oxide film whose film thickness is 5 to 15 nm and not less than that of the bottom silicon oxide film.

15. A method according to claim 12, wherein the first gate insulating film comprises a 1- to 10-nm thick bottom silicon oxide film, a film selected from the group consisting of a strontium titanate film and a barium strontium titanate oxide film as the charge storage layer, and a top silicon oxide film whose film thickness is 5 to 15 nm and not less than that of the bottom silicon oxide film.

16. A method according to claim 12, wherein the first and second gate insulating films include an HTO film as the topmost gate insulating layer.

17. A method of fabricating a nonvolatile semiconductor memory having a cell array including a cell transistor and a selection transistor, and a peripheral circuit including first and second peripheral transistors, comprising the steps of:

forming a first gate insulating film including a charge storage layer, on a surface of a semiconductor substrate, as a gate insulating film of the cell transistor;

forming a second gate insulating film not including a charge storage layer, on the surface of the semiconductor substrate, as a gate insulating film of the selection transistor;

forming a third gate insulating film not including a charge

storage layer, on the surface of the semiconductor substrate, as a gate insulating film of the first peripheral transistor;

forming a fourth gate insulating film not including a charge storage layer and thinner than the third gate insulating film, on the surface of the semiconductor substrate, as a gate insulating film of the second peripheral transistor; and

performing element isolation by forming trenches between an element region in which the cell transistor is to be formed, an element region in which the selection transistor is to be formed, and an element region in which the first and second peripheral transistors are to be formed,

wherein the step of forming the second gate insulating film and the step of forming the third gate insulating film are simultaneously performed, and the charge storage layer in the cell transistor does not exist in an element isolation region and exists only below said first gate electrode in the element region.

18. A method according to claim 17, wherein the first gate insulating film is formed by stacking a 1- to 10-nm bottom silicon oxide film, a 0.5- to 7-nm thick silicon nitride film as the charge storage layer, and a top silicon oxide film whose film thickness is 5 to 15 nm and not less than that of the bottom silicon oxide film.

19. A method according to claim 17, wherein the first gate insulating film is formed by stacking a 1- to 10-nm bottom silicon oxide film, a tantalum oxide film as the charge storage layer, and a top silicon oxide film whose film thickness is 5 to 15 nm and not less than that of the bottom silicon oxide film.

20. A method according to claim 17, wherein the first gate insulating film comprises a 1- to 10-nm thick bottom silicon oxide film, a film selected from the group consisting of a strontium titanate oxide film and a barium strontium titanate oxide film as the charge storage layer, and a top silicon oxide film whose film thickness is 5 to 15 nm and not less than that of the bottom silicon oxide film.

21. A method according to claim 17, wherein the first and second gate insulating films include an HTO film as the topmost gate

insulating layer.